AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multithreaded processor supporting a plurality of active threads, the multithreaded processor comprising:

an instruction fetch and issue unit comprising:

an instruction fetch stage configured to fetch a plurality of sets of bits, wherein each set of bits can represent a plurality of instructions; and

a pipeline coupled to the instruction fetch stage and configured to receive a set of fetched bits and an associated thread ID, wherein the pipeline comprises:

a plurality of pipeline stages, wherein each pipeline stage stores a thread ID; and

a data forwarding unit comprising a thread ID comparator, wherein the data forwarding unit is configured to forward data from a first pipeline stage having a first thread ID to a second pipeline stage having a second thread ID when the first thread ID is equal to the second thread ID, and to prevent data forwarding when the first thread ID is not equal to the second thread ID.

2. (Original) The multithreaded processor of claim 1, wherein the instruction fetch and issue unit further comprises an instruction buffer coupled to the instruction fetch stage and configured to store the sets of fetched bits and the associated thread ID for each set of fetched bits.

3. (Original) The multithreaded processor of claim 1, wherein the instruction fetch and issue unit further comprises a pre-decode stage configured to pre decode each set of fetched bits.

4-8. (Canceled)

9. (Currently Amended) ~~The~~ A multithreaded processor supporting a plurality of active threads, the multithreaded processor comprising:

an instruction fetch and issue unit comprising:

an instruction fetch stage configured to fetch a plurality of sets of bits, wherein each set of bits can represent a plurality of instructions; and

a pipeline coupled to the instruction fetch stage and configured to receive a set of fetched bits and an associated thread ID; and~~of claim 1, further comprising~~

a trap handler configured to resolve a first trap having a first thread ID when the active thread corresponds to the first thread ID, and to suspend the first trap having the first thread ID when the active thread does not correspond to the first thread ID.

10-11. (Canceled)

12. (Currently Amended) A method of operating a multithreaded processor supporting a plurality of threads, the method comprising:

fetching a first set of bits, which can represent a plurality of instructions;

attaching an associated thread ID to the set of fetched bits; ~~and~~

issuing the instructions of the first set of fetched bits with the associated thread ID to a pipeline;

storing the associated thread ID in a thread ID memory in each stage of the pipeline operating on an instruction from the first set of instructions;

forwarding data from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is equal to a second thread ID in the second pipeline stage; and

preventing data forwarding from the first pipeline stage to the second pipeline stage when the first thread ID in the first pipeline stage is not equal to the second thread ID in the second pipeline stage.

13. (Original) The method of claim 12, further comprising:

reading a first operand for the first set of instructions; and

propagating the associated thread ID through the pipeline with the first set of instructions and operand.

14-16. (Deleted)

17. (Currently Amended) ~~The~~ A method of operating a multithreaded processor supporting a plurality of threads, the method comprising:

fetching a first set of bits, which can represent a plurality of instructions;

attaching an associated thread ID to the set of fetched bits;

issuing the instructions of the first set of fetched bits with the associated thread ID to a pipeline;~~claim 12, further comprising~~

storing an active thread ID of an active thread as a trap thread ID when a trap is detected;

resolving the trap when the trap thread ID equals the active thread ID; and

preventing trap resolution when the trap thread ID does not equal the active thread ID.

18-19. (Canceled)

20. (Currently amended) A multithreaded processor supporting a plurality of threads comprising:

means for fetching a first set of bits, which can represent a plurality of instructions;

means for attaching an associated thread ID to the set of fetched bits; ~~and~~

means for issuing the instructions of the first set of fetched bits with the associated thread ID to a pipeline;

means for storing the associated thread ID in a thread ID memory in each stage of the pipeline operating on an instruction from the first set of instructions;

means for forwarding data from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is equal to a second thread ID in the second pipeline stage; and

means for preventing data forwarding from the first pipeline stage to the second pipeline stage when the first thread ID in the first pipeline stage is not equal to the second thread ID in the second pipeline stage.

21. (Original) The multithreaded processor of claim 20, further comprising:

means for reading a first operand for the first set of instructions; and

means for propagating the associated thread ID through the pipeline with the first set of instructions and operand.

22-24. (Canceled)

25. (Currently Amended) ~~The~~ A multithreaded processor supporting a plurality of threads comprising:

means for fetching a first set of bits, which can represent a plurality of instructions;

means for attaching an associated thread ID to the set of fetched bits;

means for issuing the instructions of the first set of fetched bits with the associated thread ID to a pipeline;

~~of claim 20, further comprising~~ means for storing an active thread ID of an active thread as a trap thread ID when a trap is detected;

means for resolving the trap when the trap thread ID equals the active thread ID; and

means for preventing trap resolution when the trap thread ID does not equal the active thread ID.

26-27. (Canceled)

28. (Previously Presented) The multithreaded processor of claim 1, further comprising a trace unit coupled to the instruction fetch and issue unit.

29. (Previously Presented) The multithreaded processor of claim 28, wherein the trace unit comprises:

a trace generation unit, which monitors the set of fetched bits and the associated thread ID to detect branches, jumps, or calls, and generates a program trace; and

a trace compression unit, which compresses the program trace.

30. (Currently Amended) The method of claim 12, further comprising:

monitoring the set of fetched bits and the associated thread ID to detect branches, jumps, or calls, and generates a program trace; and

compressing the program trace.

31. (Previously Presented) The multithreaded processor of claim 20, further comprising a trace unit coupled to the instruction fetch and issue unit.

32. (Previously Presented) The multithreaded processor of claim 31, wherein the trace unit comprises:

a trace generation means for monitoring the set of fetched bits and the associated thread ID to detect branches, jumps, or calls, and for generating a program trace; and

a trace compression means for compressing the program trace.